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10/677,425	10/02/2003	Robert A. Shearer	ROC920030170US1	8448

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Robert R. Williams
IBM Corporation
Dept. 917
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,425	SHEARER, ROBERT A.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because of the following reason.

All extraneous markings (such as "Atty docket No. ...") should be removed from the abstract.

Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 1-14 and 16-23 are objected to because of the following informalities:

Claims 16-23 have been renumbered 15-22, and will be referred to as such hereinafter.

As for claims 1 and 8, the words "partioning" and "re-partions" recited on lines 5 and 13 (of claim 1 – and lines 10 and 18 of claim 8) should be changed to "partitioning" and "re-partitions" respectively.

As for claims 5 and 12, the phrase "the least used buffer" recited on line 1 and "the minimum number of addressable" on line 2 should be changed to "a least used buffer" and "a minimum number of addressable" respectively to establish proper antecedent basis for these terms.

As for claim 20, the phrase "the usage" recited on line 5 should be changed to "usage".

The remaining claims are objected to for further limiting one of the previously objected to claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, one of ordinary skill in the art would be unable to

determine what exactly a "timing signal initiate" is, and further would be unable to determine how they may be used to "reset of [a] ... plurality of storage registers". It is of the examiner's opinion that Applicant intended to recite the timing signal as initiating the reset of a plurality of storage resisters. These claims will be further treated on their merits based on this assumption.

5. Claims 7 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, resetting of the storage registers is not disclosed in Applicant's specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Muller (US Patent 6,044,418).

As for claim 20, Muller teaches a method for managing a buffer comprising a plurality of addressable memory registers, comprising:

partitioning the buffer into the plurality of buffer regions controlled by hardware (col. 1, line 54 through col. 2 line 1 – the system can dynamically change the number and sizes of queues (see Fig. 4, the queue is partitioned into at least two regions, elements 425 and 430) – the partitioning is performed by hardware (i.e. state machine) – see abstract) ;

monitoring, with the hardware, the usage of each buffer region within a time period (col. 1, line 59 through col. 2, line 8 – the state machine monitors the partition pointers and determines when to resize the partitions); and

re-allocating the memory registers among the buffer regions with the hardware, based on the monitored usage (col. 1, line 59 through col. 2, line 13 – the software will reallocate based on memory usage. It is worthy to note that the hardware (state machine) is monitoring, whereas the software is reallocating).

Note, even though not recited in this claim, Muller further teaches a network switch (Fig 1, element 111) as being part of his system.

As for claim 21, Muller teaches associating each buffer region with a data class (col. 6, lines 26 through 34 – each of the partitions maintain data that is communicated through a corresponding network port. Additionally, the partitions can be either data or other information. In other words, each partition is capable of containing information or data unique to its corresponding network port (i.e. own class of data)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent 6,044,418) as applied to clam 20 above, and in further view Gil (US PG Publication 2004/0064664 A1).

As for claim 22, though Muller teaches each buffer region as storing data or information (i.e. data classes) unique to each port, he fails to specifically teach the classes as representing virtual lanes. Gil however teaches the use of virtual lanes for the ports of the HCA (paragraph 0005, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, Muller would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

8. Claims 1-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent 6,044,418) in view of Welch et al. (US Patent 6,735,633 B1)

hereinafter Welch, and in further view of Mammen (US PG Publication 2004/0047367 A1).

As for claim 1, Muller teaches a memory device, comprising:

a buffer memory having a plurality of addressable memory registers (Fig. 4 illustrates a queue with multiple registers arranged into a plurality of section or partitions);

a logic network for writing and reading data into and out of said buffer memory (Fig. 1, element 101), said logic network for partitioning said buffer memory into a plurality of buffer regions (col. 1, line 54 through col. 2 line 1 – the system can dynamically change the number and sizes of queues (see Fig. 4, the queue is partitioned into at least two regions, elements 425 and 430)), wherein said logic network writes and reads data from a plurality of data classes into said plurality of buffer regions such that each data class is written into and read from a different buffer region col. 6, lines 26 through 34 – each of the partitions maintain data that is communicated through a corresponding network port. Additionally, the partitions can be either data or other information. In other words, each partition is capable of containing information or data unique to its corresponding network port (i.e. own class of data).

Muller however fails to teach a timer sending a timing signal to recall data from a counter and repartition the buffer. It is worthy to note that Muller does teach repartitioning the buffer such that a more utilized buffer region is assigned more

addressable memory registers (col. 2, lines 9-12 - under and over utilization of the buffer regions is corrected via the resizing based on usage. In other words, assigning more registers to region that require more memory, and less to those that are under utilization their respective allocated areas).

Welch however teaches a system for bandwidth allocation in a computer network where a timer is used to time when resource reallocation is required. Once the timer is reset, it will increment between reallocation requests (col. 14, lines 21-24). Once reallocation is required the timer sends a signal to the system to indicate that reallocation is required (col. 14, lines 55-64). Subsequently, the timer will then be cleared (i.e. recalling data from the timer, which has served as a counter for the interval between reallocation (col. 14, lines 42-54)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Welsh's system for bandwidth allocation to is own system. By doing so Muller would benefit by improving the bandwidth of his own network, thereby minimizing possible data loss during packet transmissions as discussed by Welsh in col. 2, lines 12-24.

It is worthy to note that even though Muller is teaching memory allocation, and Welsh's system is for resource (i.e. bandwidth) reallocation, Welsh's system is analogous to Muller's, in that they both serve to reallocate resources over a network fabric. Welsh's teachings are introduced to show that adding a timing signal to trigger Muller's memory reallocation is an obvious variation of his presently taught system.

Muller further fails to teach incrementing a storage register every time a region reaches a predetermined usage level.

Mammen however teaches a method and system for optimizing the size of a variable buffer in which he maintains buffer read and buffer write pointers used determine if a buffer region is full. If it is determined that the buffer is full, a counter is incremented to indicate to the system that the buffer is now full (paragraph 0084, lines 17-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Mammen's system for optimizing the size of a buffer. By doing so, Muller would benefit by having a means of more effectively minimizing the depth of the buffer in his network, which in turn would produce a low delay in message transmission, hence reducing the possibility of future underflow due to packet delay variations as taught by Mammen (paragraph 0006, all lines).

As for claim 2, Muller teaches the logic network as assigning a buffer region that is used less often fewer addressable memory registers (col. 2, lines 9-12 - under and over utilization of the buffer regions is corrected via the resizing based on usage. In other words, assigning more registers to region that require more memory, and less to those that are under utilizing their respective allocated areas).

As for claim 3, Muller teaches each buffer region is always assigned at least a minimum number of addressable memory registers (this limitation is inherent as a region must contain at least one register or storage location to be

considered a valid region, therefore the minimum number of addressable registers per region is always one).

As for claim 4, Mammen teaches a method and system for optimizing the size of a variable buffer in which he maintains buffer read and buffer write pointers used determine if a buffer region is full. If it is determined that the buffer is full, a counter is incremented to indicate to the system that the buffer is now full (paragraph 0084, lines 17-24). In other words, the predetermined level is set to full as claimed by Applicant.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Mammen's system for optimizing the size of a buffer. By doing so, Muller would benefit by having a means of more effectively minimizing the depth of the buffer in his network, which in turn would produce a low delay in message transmission, hence reducing the possibility of future underflow due to packet delay variations as taught by Mammen (paragraph 0006, all lines).

As for claim 5, Muller teaches a least used buffer region is assigned the minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers (again, a memory region will always contain at least one register (minimum), yet it will always allocate more to accommodate future writes into the region).

As for claim 7, Welch teaches resetting the timer (i.e. counter) after the reallocation occurs (col. 14, lines 42-54).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Welsh's system for bandwidth allocation into his own system. By doing so Muller would benefit by improving the bandwidth of his own network, thereby minimizing possible data loss during packet transmissions as discussed by Welsh in col. 2, lines 12-24.

9. Claims 6 and 8-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Muller (US Patent 6,044,418), Welch (US Patent 6,735,633 B1) and Mammen (US PG Publication 2004/0047367 A1), and in further view of Gil (US PG Publication 2004/0064664 A1).

As for claim 8, the combined teachings Muller, Welch and Mammen meet all of the limitations of this claim with the exception of a card adaptor for transmitting and receiving data from the network switch (see the rejection of claim 1).

Gil however teaches a buffer management architecture and method for an infiniband subnetwork. In his teachings, Gil discloses an Infiniband architecture HCA card adapter in his network (paragraph 0003, all lines – see also Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, Muller would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

Claims 9-12, and 14 are similar to claims 1-5, and 7, and hence are rejected with the same rational.

As for claims 6 and 13, though Muller teaches each buffer region as storing data or information (i.e. data classes) unique to each port, he fails to specifically teach the classes as representing virtual lanes. Gil however teaches the use of virtual lanes for the ports for the HCA (paragraph 0005, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, Muller would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

As for claim 17, Gil teaches his card adaptor as a target adaptor (paragraph 0004, all lines).

As for claims 15-16 and 18-19, Gil teaches his card adaptor as a Infiniband host channel adaptor (paragraph 0005, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Muller to further include Gil's buffer management architecture into his own system of dynamically resizing queues for a network switch. By doing so, Muller would be able to exploit the benefits of an Infiniband type architecture including improved bandwidth and lower data latency over the network as described by Gil (paragraph 0003, all lines).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tremaine (US PG Publication 2004/0078532 A) teaches a system and method for dynamically allocating associative resources.

Yoshimoto et al. (US Patent 5,862,409) teach a buffer capacity change monitoring method and apparatus.

Cohen et al. (US Patent 6,230,220 B1) teach a method for allocating buffer memory.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

3/2/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER